

ABSTRACT OF THE DISCLOSURE

CPU and memory installed apparatus 101-1 through 101-3 each having CPU 103 and memory 106 and input/output control apparatus 201-1 through 201-3 are connected to each other by network 301. CPU and memory installed apparatus 101-1 has communication circuit 109 for transmitting an input/output instruction issued by CPU 103 of own CPU and memory installed apparatus to input/output control apparatus 201-1 assigned in advance to the own CPU and memory installed apparatus via network 301, and receiving a response from input/output control apparatus 201-1 via network 301. Input/output control apparatus 201-1 has communication circuit 206 for receiving an input/output instruction from CPU and memory installed apparatus 101-1 assigned in advance to own input/output control apparatus 201-1 via network 301, and transmitting a response to input/output instruction to CPU and memory installed apparatus 101-1 via network 301. When CPU and memory installed apparatus 101-1 suffers a fault and cannot be used, input/output control apparatus 201-1 is assigned to another normal CPU and memory installed apparatus 101-2.

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